Remarks

In the Office Action dated 11/28/2005 ("Office Action"), Claims 1-37 were rejected. In the Amendment set forth above, Claims 1, 12, 17, 18, 26, and 27 are amended, Claim 5 is canceled, and the remaining Claims are as originally presented. In view of the amendments to the Claims and the remarks set forth below, it is respectfully submitted that all Claims are in condition for Allowance.

1. The Specification has been corrected in the amendment set forth above to correct the title of the application from:

"System and Meth d for Detecting and Correcting Errors in a Control System" to

--"System and Method for Detecting and Correcting Errors in a Control System--.

2. Errors in the Specification will be corrected as they become known to Applicant and/or Applicant's Representative.

3. Claims 1-6, 10-17, 19 and 26-32 were rejection under 35 USC §102(b) as being anticipated by U.S. Patent No. 5, 774,648 to Kao et al. ("Kao"). This rejection is respectfully traversed.

Claim 1, as currently amended, is as follows:

A control system, comprising:

a storage device to store data signals _and a mode designator, the mode designator to select a first or a second mode of operation_;

a circuit coupled to the storage device to receive as control signals predetermined ones of the data signals _along with the mode designator_, the control signals to control operation of the circuit when the circuit is operating in the first mode; and

Error Correction Code (ECC) logic coupled to the storage device to interpret the predetermined ones of the data signals as ECC check bits to detect errors in the data signals when the circuit is operating in the second mode.

This amended Claim includes a mode designator that is stored within the storage device, and that is provided to the circuit along with the data signals. This is as shown in Applicant's Figure 4, which illustrates the ECC mode designator on line 400 being provided from control store RAM 300 together with the other data signals provided on lines 305 and 407. This designator determines whether ones of the data signals are used as control signals to control the rest of the circuit, or are used as ECC check bits. (See, for instance, Applicant's Specification page 15 line 17 et seq.)

Kao does not teach at least the following aspects of the claimed invention:

- a mode designator that is stored within a storage device (e.g., within the Kao optical disk drive, or "ODD"); and

- the mode designator is provided from the storage device along with the data signals for use in determining whether the data signals will be used for control or for error correction.

Next, the Examiner's observations regarding Claim 1 may be considered in regards to these aspects of the invention. The Examiner states that Applicant's circuit of Claim 1 is taught by the Kao ECC chip 200 and decoder logic of Figure 1 when the ECC chip is performing the data decoding operation in a "first mode". (See Office Action page 3 line 3.) The Examiner further indicates that a second Kao mode occurs when the correction mode signal is asserted to the selector 622 of Kao Figure 12 so that error correction can be performed. (See Office Action page 3, second paragraph.) In this regard, the Examiner is

equating the Kao correction mode signal of Figure 12 to Applicant's mode designator. (See, in particular, the last sentence of page 3 of the Office Action.)

The Kao correction mode signal of Figure 12 does not teach Applicant's mode designator for at least the following reasons. First, the Kao correction mode signal is *generated* by the Kao decoder *after* it has been determined that the data read from the ODD requires correction. This occurs sometime *after* the data has been read into the buffer, as described in Kao as follows:

> "A decoder 38 of the core 20 comprises a syndrome generator 40, which *detects errors* and generates syndrome bytes S(x) for each word of corrupted data *received from* the optical disk 26.....An error correcting circuit 48 uses known error locations and values to correct the errors." (Kao column 1 lines 51-54 and 64-65, emphasis added.)

Since the Kao decoder detects errors and performs correction only after data is received from the ODD, the Kao correction mode signal of Figure 12 can only be asserted after the decoder receives the data. As such, the Kao correction signal is most certainly not stored with the data on the ODD, since at that time, it is not even known whether the data is corrupted. Thus, the Kao correction mode signal cannot teach Applicant's mode designator which is stored in the storage device with the data, and is received by Applicant's circuit with the data. Moreover, nothing in Kao or the other cited references teaches or even suggests this aspect of Applicant's invention. For at least this reason, Claim 1 as currently presented, is allowable over this rejection, which should be withdrawn.

Next, the rejection of Claims 2-6 is considered. Claim 5 has been canceled. Claims 2-4 and 6 remain pending and depend from Claim 1. These Claims are allowable over this rejection for at least the reasons discussed in reference to Claim 1. These Claims further include additional aspects of Applicant's invention not taught by Kao. For example:

Claim 3 describes the aspect wherein the storage device has multiple addressable storage locations, each including a respective mode designator to control whether the circuit operates in the first or second mode for the data

signals stored at that storage location. The Examiner cites the correction mode signal of Kao Figure 12 as teaching this aspect of the invention. (See last sentence of page 3 of the Office Action.)

As discussed above, the Kao correction mode signal is generated only after the data is read from the storage device, and thus this signal is not stored within the ODD.

In addition to the foregoing, the ODD of Kao appears to be byte-addressable, since the address generator used to retrieve data from the ODD increments from 0 to a terminal value (e.g., 515) sequentially as each byte is read from the ODD to the buffer EDBF (see Kao column 8 lines 58-65). Nothing in Kao indicates that each addressable location (i.e., each byte) stores a correction mode signal of the type shown in Kao Figure 12. As stated above, storing such a signal would be impossible, since at the time the data resides on the disk, it is not yet known whether error correction operations are required for that data. For these additional reasons, Claim 3 is allowable over this rejection.

Claim 4 depends from Claim 3, and further includes using the data signals read from the storage device to generate a next address for addressing the memory. This is said to be taught by Kao column 14 lines 36-40. This passage of Kao discusses the Kao loading address generator 262 of Figure 9 that produces buffer addresses that are used by the CPU 300 and OCC 400 to access the buffer. This loading address generator uses "...a linear counter that sequentially counts the number of buffer locations from location 0 to [some end buffer location, depending on disk type]..." (Kao column 8 lines 58-65.) Two observations may be made regarding this loading address generator. First, the Kao address generation process does not appear to use any data to generate the addresses, as claimed by Applicant's Claim 4. Rather, it uses a counter that counts sequentially from 0 to a terminal address. Moreover, the Kao loading address generator appears to generate sequential byte addresses using a counter, which does not teach the aspect of generating the branch addresses of Claim 4, which by their very nature branch to some non-sequential address. For these additional reasons, Claim 4 is allowable over this rejection.

Claim 6 describes the aspect wherein the circuit includes logic to provide one or more functions of an instruction processor. This is as shown in Applicant's Figure 4. The Examiner cites column 14 lines 36-40 as teaching this aspect. As discussed above, the cited passage refers to the loading address generator 262. This address generator is not included in the Kao instruction processor (i.e., CPU 300) at all, but instead is part of the ECC chip, which includes combinational logic, but does not appear to be any sort of instruction processor as that term is used in the art. Claim 6 is allowable over this rejection for this additional reason. If this rejection is maintained, more guidance is respectfully requested regarding the relevance of the cited Kao passage in regards to Claim 6.

Next, independent Claim 12 is considered. This Claim, as currently amended, includes aspects that are similar to those discussed above in regards to Claim 1. This Claim is allowable for reasons similar to those discussed above in regards to that Claim.

Claims 13-17 and Claim 19 depend from Claim 12 and are allowable for at least the reasons discussed above in regards to Claim 1. These Claims include other aspects not taught by Kao. For example:

Claim 14 describes the aspect of Applicant's invention wherein the first signals that may be used as ECC signals are stored at the same addressable location as the data signals to be corrected. In Kao, the disks appear to be byte-addressable, as set forth in the Kao passage discussed above. The original code words and the CRC bytes of Kao, which are cited by the Examiner as teaching Applicant's first and second data signals, respectively (Office Action page 6 lines 1-2), are not stored within the <u>same addressable location</u> (i.e., the same ODD byte). Therefore, Kao does not teach this aspect of the invention, and for this additional reason, Claim 14 is allowable over this rejection.

Claim 16 describes the aspect of using the data signals to generate a next address for addressing the memory when operating in the first mode. For reasons similar to those discussed above in regards to Claim 4, this aspect of Applicant's invention is not taught by Kao.

Claim 17 describes the mode indicator as being one of the second data signals. The Examiner again cites the correction mode signal of Kao Figure 12 as teaching this aspect. (Office Action page 6 lines 10-11.) However, it may be recalled that in regards to Claim 14, the Examiner states that the second data signals are taught by the Kao CRC bytes. (Office Action page 6 line 2.) Thus, if both of the Examiner's assertions are true, and to teach all aspects of Applicant's Claim 17, the Kao correction mode signal must be stored in the ODD as one of the CRC signals. This is not the case, however. As discussed above, the Kao correction mode signal is not stored within the ODD at all, but rather is generated by the decode logic. Thus, Kao does not teach this aspect of the invention, and Claim 17 is allowable for this additional reason.

Claims 26-32 are next considered. Independent Claim 26, as amended, includes aspects that are similar to those of Claims 1 and 12, and is allowable for reasons similar to those discussed above in regards to those Claims.

Claims 27 – 32 depend from Claim 26 and are allowable for at least the reasons discussed in regards to Claim 26. These Claims include additional aspects not taught by Kao. For example:

Claim 28 describes branch means for utilizing first ones of the data signals to generate an address for the storage means. For reasons similar to those discussed above in regards to Claim 4, this aspect of Applicant's invention is not taught by Kao.

Claim 29 describes each addressable location of the memory as storing a different set of first and second ones of the data signals, wherein the first ones are check bits, and the second ones are data signals being checked with the check bits.

The Examiner's reasoning from page 6 lines 1-2 will be followed when considering Claim 29. In that reasoning, Applicant's data signals and check bits are said to be taught by the Kao codewords and CRC bytes, respectively. Therefore, for Kao to teach this aspect of Claim 29, a byte in the Kao byte-addressable ODD must store both a codeword and a CRC byte. Of course, this

is impossible, since a byte of storage is not sufficient to store both a byte of data and a CRC byte. Moreover, Kao Figure 3 and the Kao description describe that the codewords and CRC signals are never stored within a same addressable location (e.g., byte) of the ODD. (See Kao Figure 3). Therefore, this aspect of the invention is not taught by Kao, and this Claim is allowable over this rejection for this additional reason.

Claim 30 relates to the aspect wherein a respective mode designator is stored in each addressable location for the data signals stored at that location. For reasons similar to those discussed above in regards to Claims 3 and 17, this aspect is not taught by Kao.

4. Claim 18 was rejected under 35 USC §103(a) as being unpatentable over Kao. This rejection is respectfully traversed.

Claim 18 depends from Claim 12 and is allowable for at least the reasons discussed in regards to Claims 1 and 12. This Claim has been amended to clarify that the steps of Claim 18 are being performed for each of the multiple memory addresses. Based on the language of amended Claim 12, this involves reading a mode indicator and first data signals from each of the multiple memory addresses so that the steps of Claim 18 may be repeated for each of these addresses. As previously discussed, the Kao "mode indicator" (i.e., the correction mode signal) is not stored in *any* ODD storage location, let alone in multiple such locations. Thus, Kao does not teach the steps of Claim 18 wherein each of the ODD locations includes a mode indicator for use in performing the claimed method for the signals in the respective storage location. For this additional reason, Claim 18 is allowable over this rejection, which should be withdrawn.

5. Claim 22 was rejected under 35 USC §103(a) as being unpatentable over Kao in view of U.S. Patent No. 5,794,071 to Watanabe et al. ("Watanabe"). This rejection is respectfully traversed.

Claim 22 depends indirectly from Claim 12 and is allowable for at least the reasons discussed in regards to Claims 1 and 12. This Claim further describes using the second data signals as control signals to control an arithmetic logic unit (ALU) of an instruction processor.

Claim 22 depends indirectly from Claim 12. Claim 12 describes using control signals to control one or more functions of a digital system. The Examiner cites the Kao ECC chip 200 (not any CPU) as teaching Applicant's digital system that is under control of the control signals. (See, for example, Office Action page 5 line 5. Also see a similar discussion in regards to Claim 1 on page 3, line 3, which describes the ECC chip 200 as teaching Applicant's circuit.) The Kao ECC chip 200 includes encoder/decoder circuitry and some other combinational logic, as shown in Kao Figure 9. This circuit is most certainly not an instruction processor, and does not include an arithmetic logic unit.

As discussed above, Claim 22 depends indirectly from Claim 12 and further describes the digital system of Claim 12 as being an ALU of an instruction processor. The Examiner states the digital system is taught by the Kao ECC chip. Thus, for the rejection of Claim 22 to be proper, there must be some motivation to include the Watanabe ALU within the Kao ECC chip 200.

In regards to the foregoing, the Examiner states that since Watanabe generally describes the use of control signals to control an ALU of an IP, and since ALUs are recognized as an essential component of an IP, the combination of Kao and Watanabe render this aspect of the invention obvious. This reasoning does not provide any motivation for adding an ALU to the Kao ECC chip 200. The ECC chip is not an instruction processor, and there is absolutely no reason to include any aspects of an instruction processor, much less an ALU, into the Kao ECC chip 200 for encoding and decoding disk data. The Examiner is impermissible piecing together Applicant's invention in hindsight, and for this additional reason, Claim 22 is allowable over this rejection.

6. Claims 7, 20-21 and 36-37 were rejected under 35 USC §103(a) as being unpatentable over Kao in view of U.S. Patent 6,234,666 to Boone et al. ("Boone"). This rejection is respectfully traversed.

Claim 7 depends from Claim 1 and is allowable for at least the reasons discussed in regards to Claims 1. This Claim further describes a programmable storage device that is used to select the data signals that are received from the storage device for use as either control signals or ECC signals.

The Examiner cites Boone as teaching the programmable storage device described in Claim 7. Boone describes a maintenance system and interface for monitoring units within a data processing system for occurrences such as service requests, faults, timer expirations, and so on. The conditions that are to be monitored may be selected via a programmable storage device. The Boone system has nothing whatsoever to do with programmably selecting bits for use as ECC or control signals. Conversely, the Kao system has nothing to do with the Boone system for monitoring error conditions. There is no motivation to combine the maintenance system of Boone with the Kao system for encoding and decoding data for optical disks. The Examiner is impermissible piecing together Applicant's invention in hindsight.

In this regard, the Examiner states that one would be motivated to combine the programmable aspects of Boone with Kao to allow the Kao system to be multi-purpose. This is not understood. The Kao system is a specialized system adapted to encode/decode data to/from an ODD. It is not understood what other functions one skilled in the art may desire to add to the Kao system via programmability.

For at least the additional reasons set forth above, Claim 7 is allowable over this rejection, which is improper, and should be withdrawn.

Claims 20 and 21 depend from Claim 12 and are allowable for at least the reasons discussed in regards to Claims 1 and 12. These Claims further describe programmably selecting the second and first ones of the data signals, respectively, and are allowable for the additional reasons discussed above in regards to Claim 7.

PAGE 20/23 * RCVD AT 2/1/2006 3:52:38 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/24 * DNIS:2738300 * CSID:651 635 7523 * DURATION (mm-ss):08-02

Claims 36 and 37 depend from Claim 26 and are allowable for at least the reasons discussed in regards to Claims 1 and 26. These Claims further describe programmably selecting the first and second ones of the data signals, respectively, and are allowable for the additional reasons discussed above in regards to Claim 7.

7. Claims 8-9, 23-25 and 33-35 were rejected under 35 USC §103(a) as being unpatentable over Kao in view of U.S. Patent 6,708,294 to Nakao et al. ("Nakao"). This rejection is respectfully traversed.

Claims 8-9 depend from Claim 1 and are allowable for at least the reasons discussed in regards to Claims 1. These Claims further describe a parity circuit to determine whether a parity error occurred on a predetermined set of the data signals. Such parity checking is added to Applicant's system for use in situations wherein ECC checking is not utilized, as described in Applicant's Specification. (See, for example, page 14.)

The Examiner cites Nakao as teaching parity error detection. Nakao relates to a cache memory apparatus having a primary and secondary cache memory. There is no motivation to combine any aspects of this system with that of the Kao system for encoding/decoding data to/from disk.

In this regard, the Examiner states that one skilled in the art would be motivated to add the Nakao parity circuit to Kao because parity errors are widely known errors in data. This statement is not understood. Any errors in the Kao data (parity or otherwise) are detected using the RS code of the Kao redundancy bytes as follows:

> "A decoder 38 of the core 20 comprises a syndrome generator 40, <u>which detects errors</u> and generates syndrome bytes S(x) for each word of corrupted data received from the optical disk 26. The syndrome (n-k) bytes are supplied to an Euclidean operation circuit 42, which finds an error location polynomial .sigma.(x) and error value polynomial .eta.(x) using an extended Euclidean algorithm. The Euclidean operation circuit 42 is connected to an error locating circuit 44, which uses the Chien Search process to find actual error locations based on the error location polynomial .sigma.(x). The error locations, together with the error value

> polynomial .eta.(x) and error location polynomial .sigma.(x), are used by an error value calculator 46 to determine error value at each error location found by the Chien Search process. <u>An error correcting circuit 48 uses known error locations and values to correct the errors</u>. A CRC decoding circuit 50 performs CRC decoding and supplies the decoded data to the CPU 28." (Kao column 1 lines 46 – 67, emphasis added.)

Because the Kao system <u>*always*</u> detects and corrects errors in the manner described above, there is absolutely no need to add parity bits to Kao. One skilled in the art would not be motivated to add parity checking to Kao because such checking would be completely unnecessary. The Examiner is impermissibly piecing Applicant's system together in hindsight. This rejection is therefore improper, and should be withdrawn.

Claims 23-25 and 33-35 depend from Claims 12 and 26, respectively, and are allowable for at least the reasons discussed in regards to Claims 1. These Claims further describe aspects that are similar to those described above in regards to Claim 7. For the additional reasons discussed above in regards to Claim 7, these Claims are allowable over the current rejection, which is improper, and should be withdrawn.

Conclusion

In the Office Action dated 11/28/2005, Claims 1-37 were rejected. In the Amendment set forth above, Claims 1, 12, 17, 18, 26, and 27 are amended, Claim 5 is canceled, and the remaining Claims are as originally presented. In view of the amendments to the Claims and the remarks set forth herein, it is respectfully submitted that all Claims are in condition for Allowance, and a Notice of Allowance is respectfully requested. If the Examiner has any questions regarding the subject Application or this response, a call to the undersigned is encouraged and welcomed.

Respectfully submitted,

Beth L. McMahon

Beth L. McMahon
Attorney for Applicants
Reg. No. 41,987
Telephone No. (651) 635-7893

Unisys Corporation
M.S. 4773
P.O. Box 64942
St. Paul, MN 55164-0942